What is claimed is:

1. A semiconductor packaging structure for packaging a semiconductor element comprising:

a flat substrate having a chip seat and having a plurality of outer lead wires extending through lateral sides of the substrate to the bottom of the substrate;

a wall formed by molding compound and installed at periphery of the substrate so as to be formed as a groove on the flat substrate;

a liner for supporting the wall, and the liner extending inwards and outwards than the wall with a predetermined distance to prevent that a mold flush problem will induce in the wall;

bonding wires on the elements for being electrically connected to the outer circuit.

2. The semiconductor packaging structure as claimed in claim 1, wherein a transparent upper cover is installed on the element.

3. The semiconductor packaging structure as claimed in claim 1, wherein a potting resin is installed on the element.

4. The semiconductor packaging structure as claimed in claim 1, wherein the material of the substrate is selected from one of the group of BT, FR3x, FR4xx and FR5xx.

5. The semiconductor packaging structure as claimed in claim 1, wherein a mouth is installed at the inner side of the wall for indicating the mounting of the transparent upper cover.

6. The semiconductor packaging structure as claimed in claim 1, wherein the material of the liner is insulating plant.

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